Generic Reusable Hardware/Software Co-Design Implementation of a Complete FH-FSK Modem for Robust Multi-User Acoustic Underwater Communication and System Validation on a FPGA

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Abstract. Underwater communication with autonomous underwater vehicles (AUVs) has strong demands on the modems caused by the constantly changing signal propagation (multi-path propagation, scattering, diffraction and refraction at thermal layers, etc.) of the underwater channel. These demands typically lead to a modem designed to match specific conditions. This results in two major problems, first we do not want to develop for each changing environment a specific hardware and second we need a robust communication to distribute necessary information about the state of the system, current condition of the environment or to coordinate group missions. In this paper we introduced a approach to serve booth of the problems. We implemented with a flexible generic design a robust underwater communication system. The paper introduce a designed approach for a generic reusable acoustic underwater communication based on a pipelined data stream processing system on a Field Programmable Gate Array (FPGA). Exploiting the inherent synchronization mechanism of an hand-shake-based streaming bus interface to form arbitrary long pipelines composed of detached and reusable modules representing the coding and modulation algorithms without the need of an external coordination mechanism. We show that our approach is feasible, matches the problems and can easily be changed or extended to a Multiple Input Multiple Output (MIMO)-system while the recommendation on energy consumption is nearly equally and area is reduced by 45 % compared to other system implementation.

1. Introduction

Communication through a underwater channel is still a challenging field of research. Especially with small unmanned underwater vehicles, the use of electromagnetic waves is difficult to implement due the power and antenna size restrictions. Also the use of electromagnetic waves of higher frequencies, as used in terrestrial radio communications, are massively dampened by the water and thus are hard to implement considering the mentioned restrictions. Another option is a laser-based communication using Tera-hertz range. This allows high data rates for very short distances, but can only be used with a direct line of sight between the communicating underwater vehicles. A solution which has proved to be viable are acoustic waves, even for small underwater vehicles.

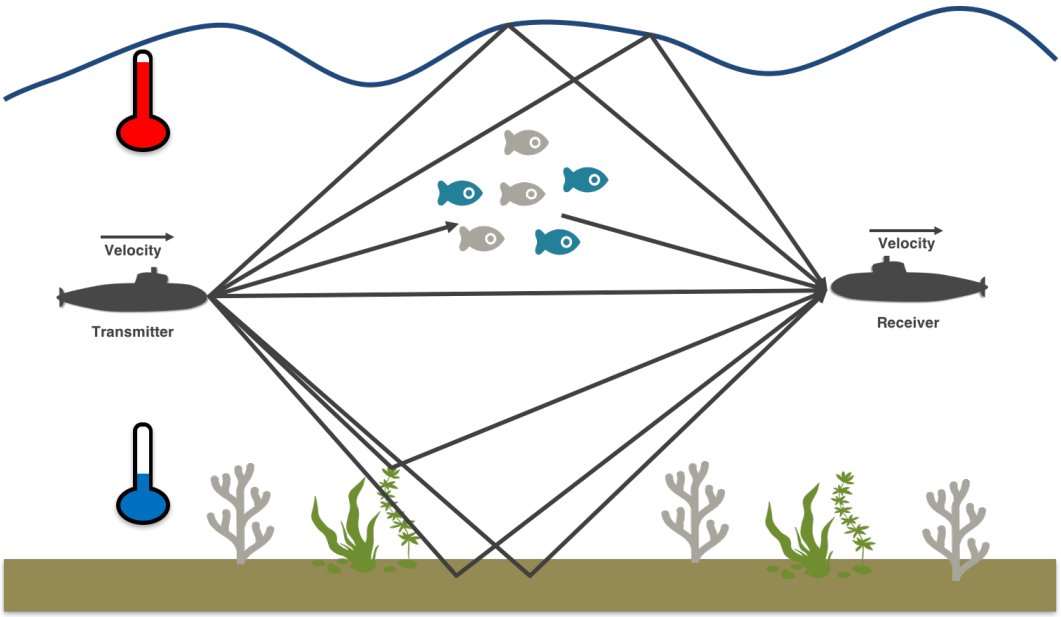

Figure 1: Schematic of the acoustic underwater channel challenge

However, the underwater channel remains quite a challenge. The channel is affected by a fast-changing multi-path propagation behavior, caused by signal scattering at the water surface, flora and fauna and the ground simplified shown in picture Figure 1. Also layers of different salinity – especially in seawater – and water temperature, in addition to phase shifts and interferences, cause refraction or even reflection. There are a lot of well-known underwater modems in research [10]-[14] and a couple of commercially underwater modems [8]-[9]. One of the most advanced modems is the Micromodem-2 [8].

But, all these developments are (i) very complex and difficult to adapt because they have been developed specifically and optimized manually or (ii) for a special task and can only be used under specific conditions. Beside the introduced problems of the underwater channel such systems like a unmanned underwater vehicle has different conditions at the modem. One of the most limited resource in a unmanned underwater vehicle is the power capacity. This leads to the need to reduce the system's energy requirements in the acDSE process and during development. Another way to reduce this consumption would be to turn down the loss rate of data.

In this work, we present a reusable generic design approach for acoustic underwater modems with focus on robust communication. As a concrete example, we implemented a fully-functional Frequency Hop-Frequency Shift Keying (FH-FSK) passband modem. The proposed approach allows us to develop the modem with respect to functional requirements and the underwater channel itself, independent of a specific target hardware. Thus, we significantly enhance usability, maintainability, extensibility, and re-usability of the modem, and benefit from a completely automatic synthesis of the high-level described modem to various target platforms. The latter particularly enables us to perform semi-automatic design space exploration, i.e., changing important parameters (water characteristics, data length, coding algorithm, carrier frequency, bandwidth, etc.) of the system and investigate the resulting quality numbers like energy-consumption or resource requirements after synthesis.

Using the generic design flow, we generated an synthesizable, testable, and configurable FH-FSK passband modem which support multiuser communication and the extension to a MIMO system. Important parameters of each variant such as the length of data, transmission frequency, bandwidth, etc. can be generic configured for each implementation and synthesized for different target platforms.

This paper is structured as follows: Section 2 introduces related work in the field of underwater communication with the focus on the robustness. Section 3 describes the proposed generic and reusable design flow and the example implementation of the complete FH-FSK band-pass modem. Section 5 presents the experimental results of our synthesized implementation compared to a model-based QPSK passband modem and the Micromodem-2 before Section 6 concludes the paper.

2. Preliminaries

The choice of the modulation method is essentially dependent on the properties of the underwater channel and the requirements of the application. In this paper, we focus on sending and receiving mission data under adverse conditions of multi-path propagation and Doppler spreads. As M. Bossert [3] has described in detail, a modulation method is used to map information in the sense of a data signal to an analog carrier signal, which can then be transmitted via the communication medium. The information can be coded either in amplitude, phase or frequency. An example of the coding in phase is Quadratur Phase Shift Keying (QPSK), while Frequency Shift Keying (FSK) maps the information into the frequency of the signal.

These basic methods can be extended or combined to improve the transmission characteristics. As explained in the essay [6], for example, Direct Sequence Spread Spectrum (DSSS) can map a symbol to a symbol sequence with good cross-correlation properties. When analyzing various methods in the work[13], some modulation methods are examined for usability in underwater communication. This compares DSSS to M - Frequency Shift Keying (MFSK) based on QPSK. MFSK works like FSK, but Mbits are encoded per symbol. Also included in the comparison is a method called Frequency-Repetition Spread Spectrum (FRSS), which works almost like DSSS, but maps the data to multiple symbols and frequencies rather than one symbol sequence, that is, a distribution in time. It has been found that none of the methods is preferable in every application.

While MFSK was the most robust against frequency shifts, FRSS had the highest performance with a low Signal to Noise Ratio (SNR). The performance of DSSS lagged behind those of MFSK and FRSS in these tests. Comparing different DSSS receivers in the work[6], on the other hand, showed that the performance of DSSS increases significantly when a dynamic chip rate adjustment is performed. The Bit Error Rate (BER) of the improved DSSS receiver in these tests was only slightly better than that of a FH-FSK receiver, while the latter is easy to implement after running [6] and possesses an intrinsic good near-far resistance, which represents an important feature for multi-user systems [15]. The higher BER can be compensated with a convolutional code after the tests [6]. The Woods Hole Oceanographic Institution (WHOI) -MicroModem 2.0 [7] uses FH-FSK for long-distance and low-speed communication. FH-FSK maps data by means of a MFSK to several carrier frequencies, which are changed periodically. Unlike FRSS, however, only one frequency is used at a given time, allowing multi-user access [4].

3. Reusable- and Generic-based Design and Development

A reusable and generic design is based on the concept of changeable components with well defined interfaces. The component itself must be adjustable and can be reached with generic parameter, which are given during the compilation process. This is comparable with concept of C++ templates. To realize such a system, the different functions of the system must be packed to in-dependable Very High Speed Integrated Circuit Hardware Description Language (VHDL) components and connect them with a well defined general interface. With the Altera-Qsys (Qsys) tool [2] we can than combine the designed components with additional peripheral like a soft-core for the used operation system, timer, internal communication interfaces, memory and so on. The basic implementation is shown schematically in Figure 5 the source code and a the documentation of the used modules and system are available for research under *Link available in the final version*. The whole system is designed to contain an arbitrary number of modules with the only condition to fully support the hand-shake-based streaming bus interface of Altera, the *Avalon Streaming Interface*. Each module contains a algorithm for the data stream manipulation to sent and provides optional parameters to define the module behavior. The Parameters are categorized in compile time and runtime parameters. While runtime parameters provide more flexibility during the use of the system compile time parameters can optimize the amount of need resources during the compilation process.

HW/SW-Codesign Architecture An important aspect of a development that must be considered is the combination of software and hardware. The flexibility of the FPGA makes it possible to develop only hardware, software only or a mix. For the first stage of development, we decided on a completely hardware-based development of the physical layer (modem) and a controller with a rudimentary communication protocol only in software. The operating system used here is the μC/OS-II. Due to the generic approach, it is always possible to move the components currently developed in hardware into the area of software. Combined with a Design Space Exploration (DSE) we are than able to find the optimum hw/sw co-design architecture/configuration depending on the limitation of the used system.

System The block diagram of the system is shown in Figure 5. Right-hand side within the dashed lines is the pipelined data stream processing with several modules. Every module is connected to its predecessor, its successor and the global system clock and reset network. Some modules which provides runtime parameters are also connected to the Memory Mapped (MM) system bus of the processor so these parameters can be distributed by software.,The data stream itself can be transported over the MM bus into the system memory by a Direct Memory Access (DMA)-Intellectual Property (IP)-Core of Altera. The concept behind this heterogeneous approach is to do all costly algorithms in the Programmable Logic (PL) of the FPGA while providing protocol handling at software level. At software level a driver is used to provide easy-to-use functions to the application layer and hide the bus transfers, configuring of the DMA-Cores and performing of a Cyclic Redundancy Check (CRC) to ensure the correct delivery of data.

MIMO The FH-FSK modem supports a multi-user access via the jump sequences. With this sequences it is possible that multiple user are able to transmit and receive data at the same time through the multiple integration of the decoder chain (see Figure 3) with different generic parameters. The automated generation of the Network-on-a-Chip (NoC) includes a generic access at this decode chains with the NIOS-II (NIOS) instance.

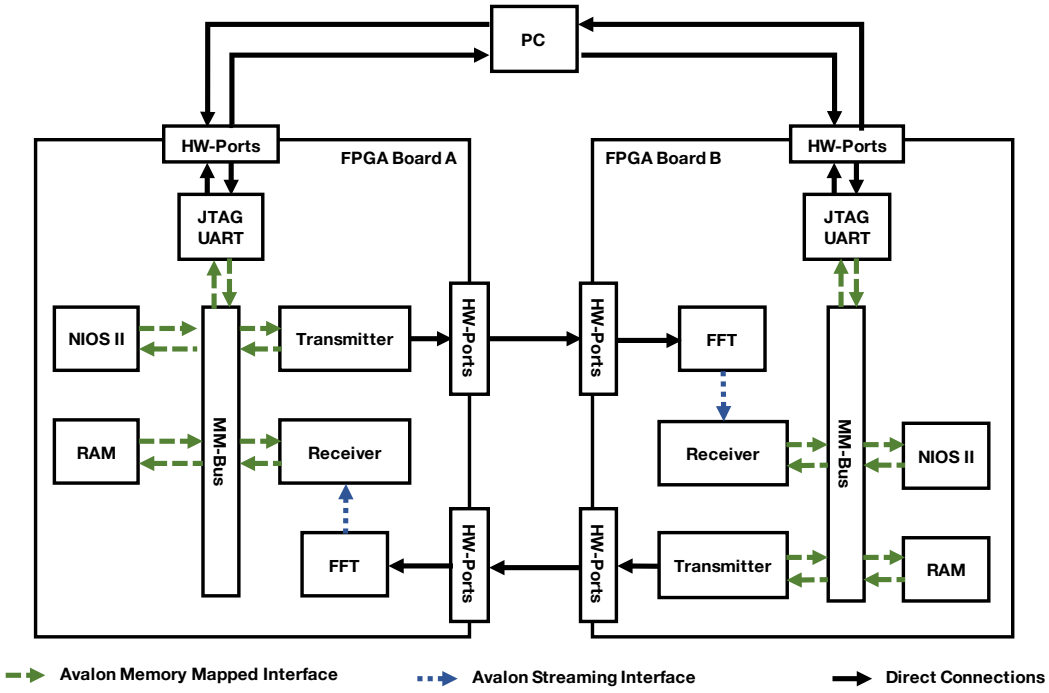

Figure 2: Schematic of two cross-connected UWMs

4. System Verification

The uniform interfaces allow the formation of arbitrary systems from the predefined modules, including those containing only the coding and the corresponding decoding component. The verification of these subsystems is possible by comparing the incoming and outgoing data stream, which must be time-delayed but otherwise identical. The concept of the subsystems is also used for the verification of the entire system (see Fig. 5). While the functionality of the individual components is checked via the tests, the interaction and timing of the communication can be assessed when considering the overall system. The test bench of the subsystems generates an input sequence with the ModelSim-Altera (ModelSim) internal random number generator, which is routed to the chain via the Avalon-Streaming (ST) interface. The test bench writes the data of the

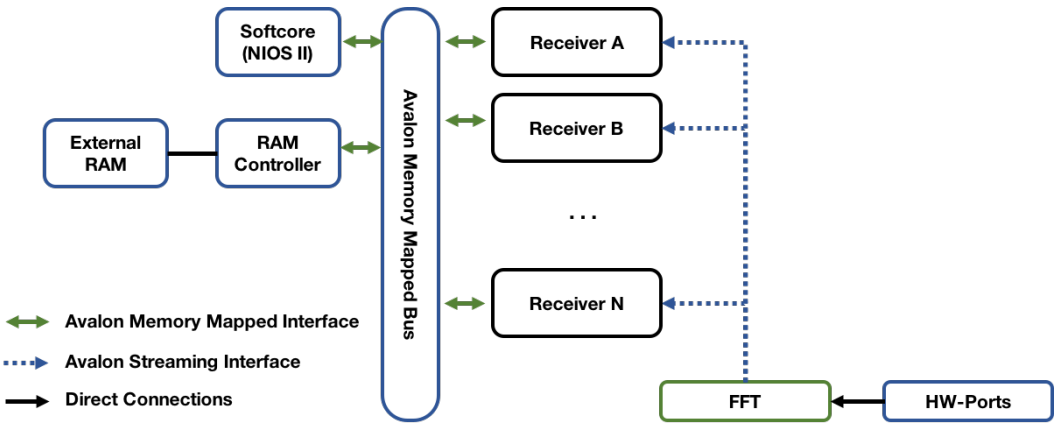

Figure 3: Schematic description of the MIMO-concept exemplary shown with the receiver

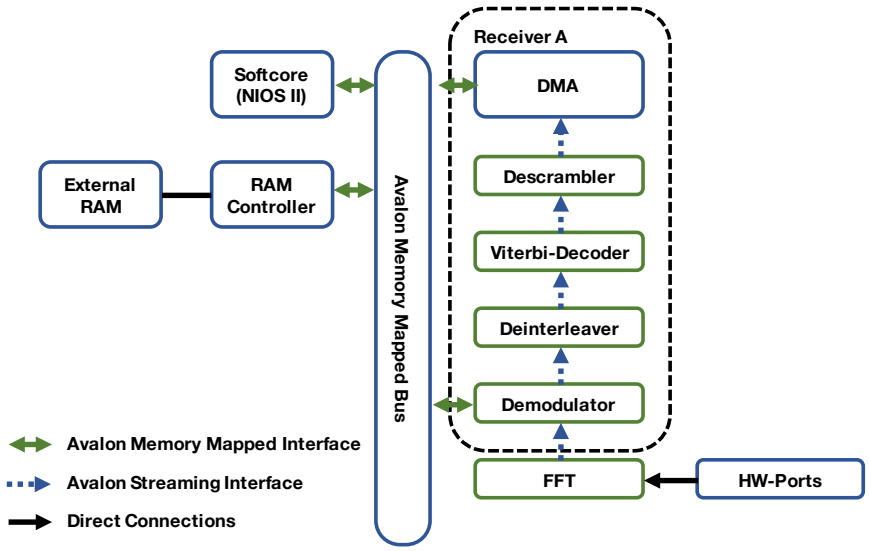

Figure 4: Architecture of the implemented pipelined data stream processing system (receiver)

two ST interfaces into a log file and will be compared with MatLab. Figure 6 shows exemplary the result of an overall test. Here you can see that an error occurs at the end of each package. This is produced by the decoding process of the convolutional code and can be corrected in post-processing. After this the sent and received data correspond to 100 %.

5. Experimental Results

After the test has been described, we discuss the resource consumption, comparing to a model-based QPSK implementation [11] and the Micromodem-2 [12] in terms of functionality and energy consumption, the development time and extensibility of the modem.

Test Settings As a test platform two Altera DE2-115 development boards were used [8]. Each has a Cyclone IV FPGA (EP4CE115F29C7) with 114,480 logic elements, 3888 kBit of on-chip memory, and four phase-locked loop (PLL) s. On each board, the system is instantiated, as shown in Figure 2. The boards are directly connected via the General Purpose Input/Output (GPIO)s. Only the modulated signal is transmitted, in the same format as given by an Analog/Digital (A/D) converter to the Fast Fourier Transform (FFT). On the NIOS a test program includes two main tasks is running on the MicroOS. The minimalistic operating system first initializes the modem, registers a function as an Interrupt Service Routine (ISR) for processing a receiving packet, and then starts the receiver.

Resource Requirements The used FPGA consists of 115 k *logic elements* (LE), which are the smallest usable unit. Furthermore, a chip can have additional functional blocks. In the case of the used Altera FPGA, there are *static random access memory* (SRAM) cells, *phase-locked loops* (PLL) and DSP blocks which consist of dedicated hard-coded multipliers. The used Altera hardware synthesis tool needs to perform a complete technology- and chip-specific traverse of the whole synthesis process to calculate the exact resource requirements. Our approach requires 23274 (20 %)bof 114480 available Logical Elements (LE). In comparison with the model-based approach

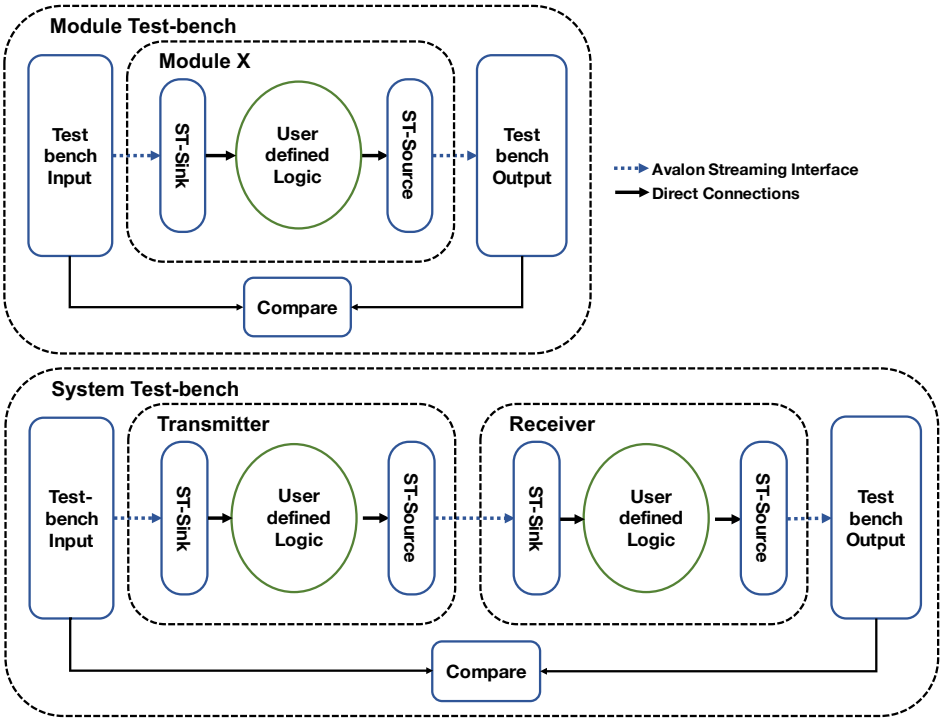

Figure 5: Schematic architecture of the test-bench implementation

(which, however, is based on QPSK and concatenated coding), we need 45 % fewer elements (see Table 1) despite the implemented soft-core except. Unfortunately there are no comparable data available for the Micromodem 2.0 [5].

Power Consumption In this work, Altera's Power-play Power Analyzer and a VCD file created by Simulink has been used to estimate the power consumption of the implemented variants. The VCD file contains time-dependent signals of the inputs and outputs for the test cases . The power consumption is calculated with a tolerance up to 20 % according to the vendor [1]. The measured values are maximums for receiving and transmitting in parallel and contains the power consumption of static-, dynamic- and I/O-components.

a) Static components: Depending on the environment, a certain amount of power will be consumed due to leakage on the FPGA during non state-changing periods.

b) Dynamic components: The dynamic power consumption is caused by the toggling of elements in the FPGA. Due to the chip's internal resistors, each change dissipates a certain amount of power.

c) In/outputs: The I/O power consumption is caused by the capacitors and resistors of the in/output pins of the FPGA.

The results in Table 1 shows that our power consumption is quite similar to the values of the other implementations at the first iteration, without optimizations or power efficient DSE. The prototype does not contain a differentiation between transmitting and receiving, which would significantly reduce the required power in the area of the dynamic components. The power consumption of

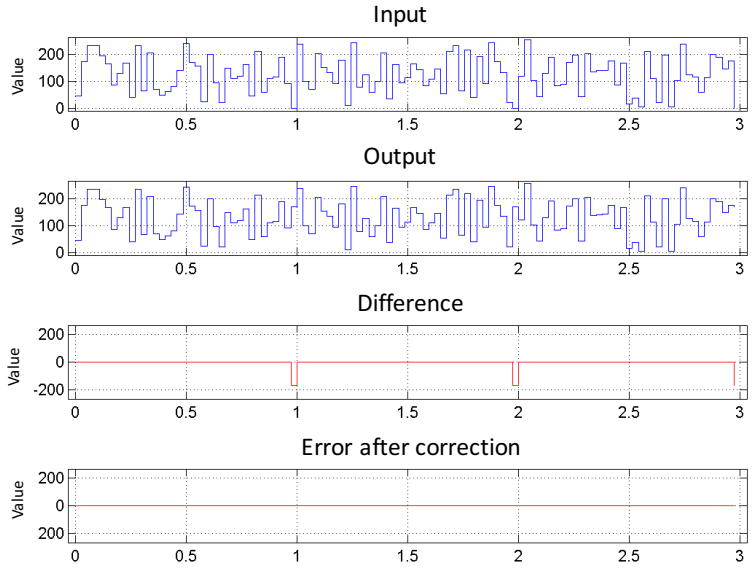

Figure 6: Section of a complete system test

Table 1: Resource utilization on a DE2-115 Development Board compared to a full model-based QPSK [11] and the WHOI Micromodem 2.0 [5] implementation

Design	Static $[mW]$	In/Out $[mW]$	Dynamic $[mW]$	Total $[mW]$	Area $[LE]$
FH-FSK	103.6	54.9	171.4	329.9	23274
QPSK RS(255,239)	101.6	42.2	116.1	259.9	42614
QPSK RS(255,239) & CC(R=1/2)	102.0	52.5	122	276.5	46535
QPSK RS(255,239) & CC(R=1/4)	102.1	48.4	131.2	281.7	49509
QPSK RS(255,223)	102.9	43.6	154.4	300.9	57878
QPSK RS(255,223) & CC(R=1/2)	103.5	54.0	182.5	340.0	65522
QPSK RS(255,223) & CC(R=1/4)	103.6	50.1	189	342.6	66481
WHOI-Micromodem-2	n.a.	n.a.	n.a.	300	n.a.

the Micromodem-2 depend on the function (transmit/receive). The variants of the implemented prototype do not differ between transmitting and receiving at this state of implementation.

Simulation Time The simulation-based verification of system is mainly characterized by its low cost and unnecessary prototypes. Furthermore, with this form of verification almost every circumstance or acceptable environmental conditions can be reproduced and analyzed. The big disadvantage here is the amount of time needed for simulation. Through the process of combining soft- and hardware components on an FPGA, we will be able to completely outsource the test as shown in Figure 7 and also to integrate the environments / channels used on hardware. By doing this, we can substantially reduce the simulation time using commercially available FPGA, taking advantage of simulation-based verification.

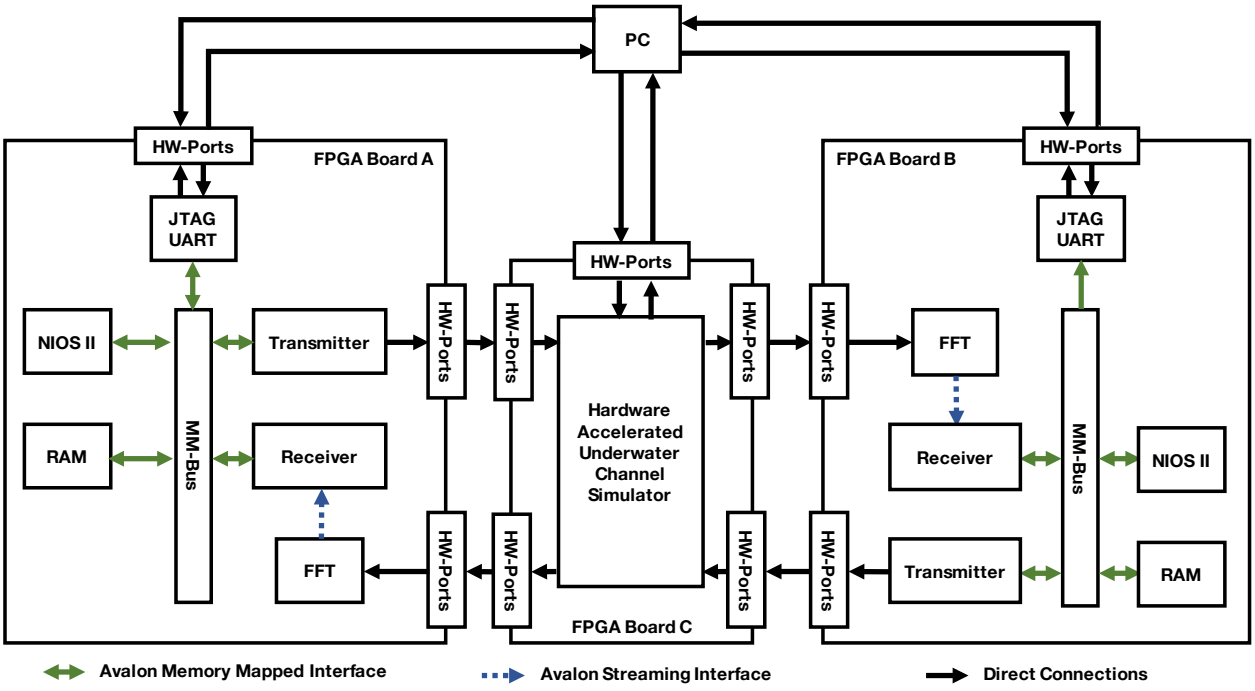

Figure 7: Schematic of two connected UWMs via a hardware accelerated UWC simulator

6. Conclusion

In summary, we have shown in this work that we can generate a reusable, partially or fully testable system by modularizing the function blocks, standardizing the interfaces and generic parameterization. This system can be simulated as well as synthesized on hardware and validated. Through this work flow, the system can be adapted easily and comprehensibly to the environment and new approaches can be checked. Furthermore, the system can be structurally extended, for example to a MIMO system. Using the HW/SW co-design, components can optionally be integrated into software and hardware and provide advanced DSE to optimize the system and allows early as the first development iteration an integration of MAC protocols and System components with access to the communication.

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